



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
[www.uspto.gov](http://www.uspto.gov)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/607,680	06/30/2000	Brad A. Barmore	042390.P8527	1233

7590                    05/08/2003

Paul A Mendonsa  
Blakely Sokoloff Taylor & Zafman LLP  
7th Floor  
12400 Wilshire Boulevard  
Los Angeles, CA 90025

[REDACTED] EXAMINER

CASIANO, ANGEL L

[REDACTED] ART UNIT      [REDACTED] PAPER NUMBER

2182

DATE MAILED: 05/08/2003

4

Please find below and/or attached an Office communication concerning this application or proceeding.

SDX

<b>Office Action Summary</b>	Application No.	SD	Applicant(s)
	09/607,680		BARMORE, BRAD A.
	Examiner	Art Unit	
	Angel L. Casiano	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) Responsive to communication(s) filed on 25 February 2003.
- 2a) This action is FINAL.                    2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_\_ is/are allowed.
- 6) Claim(s) 1-27 is/are rejected.
- 7) Claim(s) \_\_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on 30 June 2000 is/are: a) accepted or b) objected to by the Examiner.  
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) The proposed drawing correction filed on \_\_\_\_\_ is: a) approved b) disapproved by the Examiner.  
 If approved, corrected drawings are required in reply to this Office action.
- 12) The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) All b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.
- 14) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
 a) The translation of the foreign language provisional application has been received.
- 15) Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____	6) <input type="checkbox"/> Other: _____

## **DETAILED ACTION**

1. This action is in response to amendment filed 25 February 2003.
2. Claims 1-27 are pending.

### ***Drawings***

3. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "Core Logic Controller" 320 (see Figure 3). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

4. Claim objections have been overcome with the corrections filed in the amendment.

### ***Claim Rejections - 35 USC § 112***

5. Rejections under 35 U.S.C. 112 have been overcome with the corrections filed in the amendment.

### ***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 1-2, 4-11, 13-20, and 22-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pecone [US 5,604,871].
8. Pecone [US 5,604,871] was cited as prior art in the previous office action. The rejections are respectfully maintained and repeated as set forth below.

Regarding Claim 1, Pecone discloses a system comprising a motherboard (column 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having the desired interface and logic circuits (column 2, lines 53-54). Although the reference does not explicitly mention a chipset, it would have been obvious to one of ordinary skill in the art the term “chipset” refers to integrated circuits designed to perform one or more functions. The reference also discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (column 3, lines 42-44). Accordingly, Pecone also teaches a riser card coupled with the motherboard (column 7, lines 1-4; lines 34-38), having a circuit (column 4, line 67; column 5, lines 2-5; column 3, line 35) that interacts with a portion of the chipset to provide a functionality (column 3, line 37) having a memory (column 3, line 32) to store one or more indications of the functionality. However, although Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications, it would have been obvious to modify the disclosure in order to include a driver. It is well known in the art that a driver is a code that works to communicate an operating system and a

peripheral. Being a riser card part of the hardware, it would have been obvious to include a driver that would specifically load the required code in order to make the claimed system functional.

As for Claim 2, the reference includes a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see column 8, lines 13-17; column 7, lines 34-38; column 2, lines 65-67; column 3, lines 1-3).

As for Claims 4-8, the claimed functionalities constitute examples of the possible applications of the system disclosed by Pecone, as explained related to claim 1. Therefore, these claims are rejected under the same rationale.

As for Claim 9, Pecone does not include a sequence of instructions to cause a driver to be loaded. Nonetheless, it would have been obvious at the time the invention was made, since a riser card is part of the hardware, to include a driver that would specifically load the required code in order to make the system functional.

Regarding Claim 10, Pecone teaches a system comprising a motherboard (column 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having the desired interface and logic circuits (column 2, lines 53-54). Although the reference does not explicitly mention a coupled “chipset”, it would have been obvious to one of ordinary skill in the art that the term “chipset” implies integrated circuits designed

to perform one or more functions. This term is commonly used in reference to the core functionality of the motherboard. The reference discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (column 3, lines 42-44; lines 59-62). Accordingly, Pecone teaches a riser card coupled with the motherboard (column 7, lines 1-4; lines 34-38), having a circuit (column 4, line 67; column 5, lines 2-5; column 3, line 35) that interacts with a portion of the chipset to provide a functionality (column 3, line 37) and also having a memory (column 3, line 32) to store one or more indications of the functionality. However, although Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications, it would be obvious to modify the disclosure in order to include a driver, since a driver is a code that works to communicate an operating system and a peripheral. It would have been obvious to one of ordinary skill in the art, since a riser card is part of the hardware, to include a driver that specifically loads the required code in order to make the claimed riser card functional.

As for Claim 11, the reference teaches a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see column 8, lines 13-17; column 7, lines 34-38; column 2, lines 65-67; column 3, lines 1-3; column 5, lines 6-7).

As for Claims 13-17, these limitations (audio codec, modem codec, USB support, SMBus device support, and networking functionality) constitute examples of possible

applications of the riser card disclosed by Pecone, as explained on claim 10. Therefore, these claims are rejected under the same rationale.

As for Claim 18, Pecone does not explicitly disclose a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the disclosure in order to include a driver because this is a code that works to communicate an operating system and a peripheral. Thus, it would have been obvious to someone with ordinary skill in the art to include a driver that would specifically load the required code in order to make the riser card functional.

Regarding Claim 19, the reference discloses a memory, intended to store a sequence of instructions, coupled with the motherboard (column 3, lines 42-44), as claimed. The reference also discloses a system comprising a motherboard (column 2, lines 49-50) coupled to data, address, control, power and ground signals, as well as a riser card having the desired interface and logic circuits (column 2, lines 53-54). Although the reference does not explicitly mention a “chipset”, as it is well known in the art, the term “chipset” refers to integrated circuits designed to perform one or more functions. This term is commonly used in reference to the core functionality of the motherboard.

As for Claim 20, Pecone includes a riser card coupled with the motherboard via a slot interface having pins corresponding to one or more predetermined standards (see column

8, lines 13-17; column 7, lines 34-38; column 2, lines 65-67; column 3, lines 1-3), as claimed.

As for Claims 22-26, the claimed limitations (audio codec, modem codec, USB support, SMBus device support, and networking functionality) constitute examples of possible applications of the memory disclosed by Pecone, as explained on claim 19. Therefore, these claims are rejected on the same basis.

As for Claim 27, the cited reference does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications. Nonetheless, it would have been obvious to modify the disclosure in order to include a driver. It is well known in the art that a driver is a code that works to communicate an operating system and a hardware device. Therefore, being a memory a hardware device, it would have been obvious to one of ordinary skill in the art to include a driver that would specifically load the required code in order to make it functional.

9. Claims 3, 12, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Pecone [US 5,604,871] in view of the technical disclosure by IBM (*Enhanced Riser Card with Expansion Function Capability for Personal Computer*, Technical Disclosure Bulletin, July 1994).

10. IBM (*Enhanced Riser Card with Expansion Function Capability for Personal Computer*, Technical Disclosure Bulletin, July 1994) was cited as prior art in the previous office action. The rejections are respectfully maintained and repeated as set forth below.

As for Claim 3, Pecone does not specify the memory of the riser card in the claimed as ROM. It is not disclosed either a BIOS boot sequence. However, the technical disclosure discusses expanding the functionality of a riser card by including a Basic Input/Output Software (BIOS) and a Read-Only Memory (ROM). It is obvious that this disclosure suggests improving the system disclosed by Pecone by adding a BIOS and a ROM to the riser card. Accordingly, it would have been obvious to one of ordinary skill in the art to combine the references in order to obtain a low-cost versatile system.

As for Claim 12, Pecone does not specify the memory of the claimed riser card as ROM. It does not disclose either a BIOS boot sequence. However, the IBM disclosure teaches expanding the functionality of a riser card by including a Basic Input/Output Software (BIOS) and a Read-Only Memory (ROM). It is obvious that the disclosure suggests the improvement of the disclosed riser card by Pecone by the addition of a BIOS and ROM. Therefore, it is obvious that one of ordinary skill in the art would have been motivated to modify the cited reference in order to include the ROM and BIOS in the riser card, given the benefits in terms of economic factors and upgrading convenience.

As for Claim 21, Pecone does not specify the memory comprising an interface to couple to a riser card as ROM. However, the technical disclosure by IBM discusses expanding the functionality of a riser card by including a Read-Only Memory (ROM). It is obvious that this disclosure suggests improving the system disclosed by Pecone by adding a ROM coupled to the riser card. This improvement is obvious given the benefits of the modification in terms of economy and technical upgrading.

*Response to Arguments*

11. Applicant's arguments filed 25 February 2003 have been fully considered but they are not persuasive.
12. In the remarks, applicant argued in substance that Pecone [US 5,604,871] does not disclose a sequence of instructions to cause a driver to be loaded, at least in part, on one or more indications of functionality.
13. In response to applicant's arguments, Pecone teaches a memory that stores a sequence of instructions, coupled to the motherboard (column 3, lines 42-44). Pecone also teaches a riser card coupled with the motherboard (column 7, lines 1-4; lines 34-38), having a circuit (column 4, line 67; column 5, lines 2-5; column 3, line 35) that interacts with a portion of the chipset to provide functionality (column 3, line 37). The memory in the cited disclosure (column 3, line 32) stores one or more indications of the functionality. Accordingly, although Pecone does not include a sequence of instructions to cause a driver to be loaded based, at least in part, on the one or more indications, it would have been obvious to modify the disclosure in order to include a driver. It is well known in the

art that a driver is a code that works to communicate an operating system and a peripheral. It is well known in the art that a riser card is part of the hardware and therefore it would have been obvious to include a driver that would specifically load the required code in order to make the claimed system functional. It is known in the art that a driver is a routine that links the operating system and the peripheral device. A driver contains the necessary machine code to perform the function requested by an application. The operating system calls the driver when this is added to the computer system. Therefore, in order to have a functional driver, a sequence of instructions would have been necessary, and thus, obvious in order to allow the driver to be loaded. Examiner respectfully responds that a reference is to be considered not only for what it expressly states, but for what it would reasonably have suggested to one of ordinary skill in the art.

In re DeLisle, 160 USPQ 806 (CCPA 1969).

### *Conclusion*

14. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Lash et al. [US 6,363,450 B1] discloses a memory riser card for a computer system
- Kim [US 5,961,618] teaches a dual-bus riser card for an expansion slot
- Desai [US 5,765,008] discloses a personal computer with riser card PCI and Micro Channel Interface
- Liu et al. [US 6,345,072 B1] discusses a universal DSL link interface between a DSL digital controller and a DSL codec.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel L Casiano whose telephone number is 703-305-8301. The examiner can normally be reached on 830-500pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey Gaffin can be reached on 703-308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7239 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Application/Control Number: 09/607,680  
Art Unit: 2182

Page 12

alc  
May 5, 2003

  
JEFFREY GAFFIN  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100  
JEFFREY GAFFIN